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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,853	01/11/2002	Steven Teig	SPLX.P0007	9148

23349 7590 03/02/2004

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,853	TEIG ET AL.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *36-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/043853 Attorney's Docket #: SPLX.P0007
Filing Date: 1/11/2002;

Applicant: Steven et al.

Examiner: Alexander Williams

This application is a continuation of 09/681776, filed 6/3/2001 which is a continuation of 09/733104, filed 12/7/2000.

Applicant's Amendment in Paper # 5, filed 1/3/03 has been acknowledged.

Claims 1-35 and 42-47 have been canceled.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the integrated circuit comprising: at least one metal layer comprising at least two pairs of conductors to interconnect one or more points on the integrated circuit, wherein a conductor comprises one or more wires and a wire comprises a continuous segment deposed in a single direction, each pair of conductors comprising: a first wire deposed in a first Manhattan direction relative to the boundaries of the integrated circuit, the first wire comprising a first wire length including first and second ends; a second wire deposed in a second Manhattan direction relative to the boundaries of the integrated circuit, the first Manhattan direction being different than the second Manhattan direction, the second wire comprising a second wire length including first and second ends, the first end of the second wire being coupled to the second end of the first wire in claim 36, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claims 36 to 41 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 36, is unclear and confusing to what is meant and what shows "integrated circuit comprising: at least one metal layer comprising at least two pairs of conductors to interconnect one or more points on the integrated circuit, wherein a conductor comprises one or more wires and a wire comprises a continuous segment deposed in a single direction, each pair of conductors comprising: a first wire deposed in a first Manhattan direction relative to the boundaries of the integrated circuit, the first wire comprising a first wire length including first and second ends; a second wire deposed in a second Manhattan direction relative to the boundaries of the integrated circuit, the first Manhattan direction being different than the second Manhattan direction, the second wire comprising a second wire length including first and second ends, the first end of the second wire being coupled to the second end of the first wire." Where is this structure shown in the drawings?

Any of claims 36 to 41 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> **(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 36 to 39 and 41, insofar as they can be understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Jones et al. (U.S. Patent # 5,980,093).

36. Jones et al. (figures 1 to 9E) specifically figure 7C show a package enclosing an integrated circuit comprising: at least one metal layer **(102,104,106)** comprising at least two pairs of conductors to interconnect one or more points on the integrated circuit, wherein a conductor comprises one or more wires and a wire comprises a continuous segment deposed in a single direction, each pair of conductors comprising:
a first wire deposed in a first Manhattan direction **106** relative to the boundaries of the integrated circuit, the first wire comprising a first wire length including first and second ends; a second wire deposed in a second Manhattan direction relative to the boundaries of the integrated circuit, the first Manhattan direction being different than the second Manhattan direction **104**, the second wire comprising a second wire length including first and second ends, the first end of the second wire being coupled to the second end of

the first wire; and wherein, an effective wiring direction of the pairs of conductors comprises an angle, A, measured relative to the boundaries of the integrated circuit, defined by the expression Tan A = Y/X, wherein, Y comprises a line segment with a distance starting from the second end of the second wire in the last conductor pair and ending at an intersection with a line segment propagated from the first end of the first wire and in the direction of the first wire, and X comprises a distance, measured in the direction of the first wire, starting from the first end of the first wire and ending with the intersection of the Y line.

37.The integrated circuit as set forth in claim 36, the combination with Jones et al.'s first Manhattan direction comprises a horizontal direction and the second Manhattan direction comprises a vertical direction.

38.The integrated circuit as set forth in claim 36, the combination with Jones et al.'s first Manhattan direction comprises a vertical direction and the second Manhattan direction comprises a horizontal direction.

39.The integrated circuit as set forth in claim 36, the combination with Jones et al.'s first wire length equals the second wire length so as to simulate an effective direction of 45 degrees.

41.The integrated circuit as set forth in claim 36, the combination with Jones et al.'s metal layer comprises a plurality of independent conductors deposed in parallel.

Claim 40 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Jones et al. (U.S. Patent # 5,980,093) in view of Funaki et al. (U.S. Patent # 5,980,093).

Jones et al. Show the features of the claimed invention as detailed above, but fail to explicitly show the ratio of the first wire, length to the second wire length equals three to two, so as to simulate an effective wiring direction of 60 degrees.

Funaki et al. is cited for showing a MOS Gate type semiconductor devices. Specifically, Funaki et al. (figures 1 to 23) discloses the ratio of the first wire, length to the second wire length equals three to two, so as to simulate an effective wiring direction of 60 degrees (see column 12, lines 1-45) for the purpose of decreasing resistance in contact regions.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Fanaki et al.'s wiring directon of 60 degrees to modify Jones et al.'s wire direction for the purpose of decreasing resistance in contact regions.

Claims 36 to 41, insofar as they can be understood, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Glenn (U.S. Patent # 6,150,193) in view of Igarashi et al. (U.S. Patent # 6,262,487 B1).

36. Glenn (figures 1 to 20) specifically figure 7-9 and 13b show a package enclosing an integrated circuit comprising: at least one metal layer **50** comprising at least two pairs of conductors **26** to interconnect one or more points on the integrated circuit, wherein a conductor comprises one or more wires and a wire comprises a continuous segment deposed in a single direction, each pair of conductors comprising:
a first wire deposed in a first Manhattan direction relative to the boundaries of the integrated circuit, the first wire comprising a first wire length including first and second ends; a second wire deposed in a second Manhattan direction relative to the boundaries of the integrated circuit, the first Manhattan direction being different than the second Manhattan direction, the second wire comprising a second wire length including first and second ends, the first end of the second wire being coupled to the second end of the first wire; and wherein, an effective wiring direction of the pairs of conductors comprises an angle, A, measured relative to the boundaries of the integrated circuit (figure 8C), defined by the expression Tan A = Y/X, wherein, Y comprises a line segment with a distance starting from the second end of the second wire in the last conductor pair and ending at an intersection with a line segment propagated from the first end of the first wire and in the direction of the first wire, and X comprises a distance, measured in the direction of the first wire, starting from the first end of the first wire and ending with the intersection of the Y line segment **(see column 7, line 39 to column 9, line 8) (see figures 7C and 8C)**. Glenn fails to explicitly show the integrated circuit. However, it would be obvious to one of ordinary skill in the art to have an integrated circuit in the semiconductor device package.

Igarashi et al. is cited for showing a semiconductor integrated circuit device. Specifically, Igarashi et al. (figures 1 to 29) specifically figure 5 discloses the internal structure of a semiconductor device's integrated circuit for the purpose of forming a X-Y reference wiring grid using wirings of metal layers.

37.The integrated circuit as set forth in claim 36, the combination with Glenn's first Manhattan direction comprises a horizontal direction and the second Manhattan direction comprises a vertical direction.

38.The integrated circuit as set forth in claim 36, the combination with Glenn's first Manhattan direction comprises a vertical direction and the second Manhattan direction comprises a horizontal direction **(see figures 7c and 8c)**.
39.The integrated circuit as set forth in claim 36, the combination with Glenn's first wire length equals the second wire length so as to simulate an effective direction of 45 degrees **(see figures 7c and 8c)**.
40.The integrated circuit as set forth in claim 36, the combination with Glenn's ratio of the first wire, length to the second wire length equals three to two, so as to simulate an effective wiring direction of 60 degrees **(see figures 7c)**.
41.The integrated circuit as set forth in claim 36, the combination with Glenn's metal layer comprises a plurality of independent conductors deposed in parallel.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Igarashi et al.'s integrated circuit to modify Glenn's package enclosing an integrated circuit for the purpose of forming a X-Y reference wiring grid using wirings of metal layers.

Response

Applicant's arguments filed 11/17/03 have been fully considered, but are moot in view of the modified and new grounds of rejections detailed above.

Applicant's arguments are not to be persuasive. The Examiner does not agree with the argument that "Glenn's invention concerns a package, not an integrated circuit." Webster's II New Riverside University Dictionary define "integrated circuit" is a tiny complex of electronic components and their connections that is produced in or on a small slice of material. Figures7-9, and 13b of Glenn show a device having tiny complex of electronic through holes 14, contacts 27, ends 26a and balls 28, which are absolutely electronic components, and also metallization connections between ends 26a and ball 28. These electronic components and connections are produced in and on a small slice of material 13. Therefore, by definition of Webster's II dictionary, the device as shown in figures 7-9 and 13b of Glenn is an integrated circuit.

Further, the limitation "wherein, an effective wiring direction of the pairs of conductors comprises an angle, A, measured relative to the boundaries of the integrated circuit, defined by the expression Tan A = Y/X, wherein, Y comprises a line segment with a distance starting from the second end of the second wire in the last conductor pair and ending at an intersection with a line segment propagated from the first end of the first wire and in the direction of the first wire, and X comprises a distance, measured in the direction of the first wire, starting from the first end of the first wire and ending with the intersection of the Y line segment" has been held that the functional

"wherein" statement does not define any structure and accordingly can not serve to distinguish. In re Mason, 114 USPq 127, 44 CCPA 937 (1957).

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/776,773,758,200,668,670,700,778,775,211,210,208, 207,206,208,72,401,369,315,300,209 716/7,1,12,7,5,8,1-21 361/735 345/443 438/197,33,113 29/850	6/28/03 2/20/04
Other Documentation: foreign patents and literature in 257/776,773,758,200,668,670,700,778,775,211,210,208, 207,206,208,72,401,369,315,300,209 716/7,1,12,7,5,8,1-21 361/735 345/443 438/197,33,113 29/850	6/28/03 2/20/04
Electronic data base(s): U.S. Patents EAST	6/28/03 2/20/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
2/20/2004

Alexander Williams
Primary Examiner